(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 January 2002 (03.01.2002)

PCT

(10) International Publication Number
WO 02/01735 A2

(51) International Patent Classification[7]: H04B

(21) International Application Number: PCT/US01/19907

(22) International Filing Date: 21 June 2001 (21.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/603,310 21 June 2000 (21.06.2000) US

(71) Applicant: PULSE-LINK, INCORPORATED [US/US]; Suite 8., 9155 Brown Deer Road, San Diego, CA 92121 (US).

(72) Inventors: **SPARRELL, Carlton**; 2100 Oberlin Street, Palo Alto, CA 94306 (US). **AIELLO, Roberto**; 470 Alger Drive, Palo Alto, CA 94306 (US). **ROGERSON, Gerald**; 2204 Hermosa Court, Morgan Hill, CA 95037 (US). **HO, Minnie**; 3427 Thomas Drive, Palo Alto, CA 94303 (US).

(74) Agent: D'ALESSANDRO, Kenneth; Sierra Patent Group, Ltd., P.O. Box 6149, Stateline, NV 89449 (US).

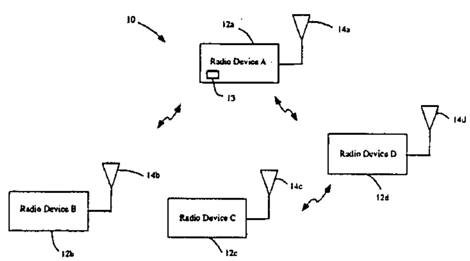
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *without international search report and to be republished upon receipt of that report*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: WIRELESS TDMA SYSTEM AND METHOD FOR NETWORK COMMUNICATIONS




WO 02/01735 A2

(57) Abstract: The present invention describes a network communication system which includes a first slave transceiver configured to communicate a plurality of TDMA data packets at different data rates to a second slave transceiver. The second slave transceiver is also configured to communicate a plurality of TDMA data packets at different data rates to the first slave transceiver. A master transceiver manages data communications between the first slave transceiver and the second slave transceiver. Each transceiver includes a data modulation unit, a transmitter, an antenna, and a receiver. The data modulation unit is configured to generate a plurality of signals having variable pulse repetition frequencies and different modulation techniques. The transmitter is coupled to the data modulation unit and the transmitter is configured to generate a pulse stream according to the data modulation unit. The transmitting antenna is coupled to the transmitter and the transmitting antenna is configured to transmit a plurality of ultra wide band baseband signals. The receiver is configured to detect and demodulate said ultra wide band base band signals operating at variable pulse repetition frequencies and having different modulation methods.



# SPECIFICATION

# WIRELESS TDMA SYSTEM AND METHOD FOR NETWORK COMMUNICATIONS

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to wireless network communications. More particularly, the present invention relates to a Time Division Multiple Access (TDMA) system and method

### 2. The Background Art

Time Division Multiple Access (TDMA) is well known in the art as a method of utilizing bandwidth across a shared medium. The basic principle of time division multiplexing is that it permits a user to have access to a TDMA system which operates at a rate which is several times greater that the rate required to support the user's own data throughput.

Several common wireless protocols employ TDMA, such as the Global Mobile System (GSM), Digital Enhanced Cordless Telecommunications (DECT), and Bluetooth. GSM is a European standard which employs simultaneous TDMA and Frequency Division Multiple Access (FDMA) schemes in which each frequency used for communication is divided into TDMA slots. With GSM each TDMA device is assigned slots for transmit, receive and base station communications. All GSM communications in the system take place using the Gaussian Minimum Shift Keying (GMSK) modulation technique.

DECT is a standard developed by the European Telecommunication Standard Institute for use in European digital mobile telephone systems. DECT uses frames of 24 slots allowing up to 12 channels for transmit and 12 channels for receive. Each device on the DECT network uses the same modulation technique, but the system allocates varying bandwidth to devices by assigning multiple slots or through the use of padding to stretch packets to uniform lengths.

Bluetooth is a technology specification for small form factor, low-cost, short range radio links between mobile PCs, mobile phones and other portable devices. Additionally, Bluetooth is an emerging standard for consumer wireless devices which uses TDMA. Under this standard, devices can be assigned one or more 625$\mu$s time slots in which to transmit or receive. Each device uses the same modulation technique. Different bandwidth devices are accommodated by assigning multiple contiguous timeslots to devices with increased throughput requirements.

For each of the wireless protocols described above, a common modulation scheme is employed by all devices on the network. Additionally, a common wireless

medium is allocated to devices with different bandwidth requirements to share the same network. Furthermore, in each of the previously described protocols, increased bandwidth demands for high bit-rate devices are satisfied by assigning longer time slots to the high bandwidth device. Low bit-rate devices are accommodated by allowing them to zero-fill assigned slots up to the minimum slot length supported.

Therefore, it would be beneficial to allow devices with different bit-rates to communicate with one another. Previous systems have been employed where a TDMA scheme allows different devices to be assigned different time slots at different bit-rates.

United States Patent 4,201,892 ('892) titled "Multi-Rate TDMA Communication System" is one system developed for satellite communications in which two different bit-rates are supported in the same TDMA frame using two different frame reference bursts. At the beginning of each frame, the primary frame reference burst is transmitted followed by one or more time-slots assigned to devices capable of communicating using the primary bit-rate. After the primary bit-rate slots, a device synchronized to the primary frame reference burst transmits a secondary frame reference burst at a secondary bit-rate. Devices capable of transmitting at the secondary bit-rate are then allowed to transmit slots following the secondary frame reference burst. The system is configured so that the secondary slots are completed before the next primary frame reference which begins the following frame.

This system and method of interleaving two or more classes of different bit-rate devices has limited application for a variety of reasons. For example, the system requires multiple frame reference bursts and divides the frame into separate sections isolated by these frame reference bursts. It would therefore be beneficial to provide a system that does not require multiple frame reference bursts and allows devices of varying bit-rates to be assigned slots at any point within the frame. By allowing devices to be assigned slots anywhere within the frame, there is greater flexibility when devices of different bandwidths are continuously signing one and off from the network.

United States Patent 4,586,177 ('177) titled "Integrated Narrowband and Wideband TDMA Networks" is another teaching which allows different devices to be assigned different time slots at different bit-rates. Like the '892 patent, the network system provides that different reference bursts are used to divide the frame into sub-frames supporting devices of differing bit rates. However, unlike the '892 patent, the system disclosed in the '177 patent divides the frame to support two types of devices. The system supports wideband devices which are assigned the complete bandwidth during TDMA slots as well as narrowband devices which share the bandwidth during TDMA slots using a FDMA technique.





However, the network system disclosed in the '177 patent is limited to the use of multiple frame reference bursts. Additionally, the patent is limited to devices having specific bit-rates beings assigned slots following their respective reference bursts. Further still, each of these bursts are transmitted at a different carrier frequencies.

Another system in the prior art is described in "A Time Division Multiple Access System for the Defense Satellite Communication System" by Husted and Walker, appearing in the reports of the 1970 EASCON, pages 229-237. This system uses an external timing source for framing information and does not use a frame reference burst.

The limitation of Husted et al.'s TDMA Sattellite Communication System is that any device participating in this system must be capable of demodulating the highest bit rate signal. Therefore, the low bit-rate devices must include all electronics and timing necessary to receive at the higher bit-rate and prevents low-cost, low bit-rate devices from being developed.

Therefore, it would be beneficial to provide a network which would allow low bit rate devices to communicate with high bit rate devices.

It would also be beneficial to provide a system and method for devices operating with different modulation methods to communicate with one another.

Further still it would be beneficial to provide a system and method wherein a master device synchronizes the communications between slave devices, and the communications may be accomplished by varying the pulse repetition frequency, the modulation technique, the TDMA frame slot size, and the number of slots in a TDMA frame.

## SUMMARY OF THE INVENTION

The present invention describes a network communication system which includes a first slave transceiver configured to communicate a plurality of Time Division Multiple Access (TDMA) data packets at different data rates to a second slave transceiver. The second slave transceiver is also configured to communicate a plurality of TDMA data packets at different data rates to the first slave transceiver. A master transceiver manages data communications between the first slave transceiver and the second slave transceiver.

Each transceiver includes a data modulation unit, a transmitter unit, an antenna, and a receiver. The data modulation unit is configured to generate a plurality of signals having variable pulse repetition frequencies and different modulation techniques. The transmitter unit is coupled to the data modulation unit and the transmitter unit is configured to generate a pulse stream according to the data modulation unit. The transmitting antenna is coupled to the transmitter unit and the transmitting antenna is configured to transmit a plurality of ultra wide band base band

signals. The receiver is configured to detect and demodulate the ultra wide band base band signals operating at variable pulse repetition frequencies and having different modulation methods.

The present invention provides a system and method for low bit-rate devices to communicate with high bit-rate devices. The present invention also provides a system and method for devices operating with different modulation techniques to communicate with one another. The present system and method provides a TDMA system and method that allows sharing a wireless medium with devices capable of transmitting and receiving at different data rates. The system and method are particularly applicable to base band spread spectrum networks, also referred to herein as ultra-wide band networks.

The system of the preferred embodiment comprises a network of transceiver node devices. Each transceiver transmits and receives data. In the preferred embodiment, the invention provides data transmission with base band wireless technology which is also referred to as ultra wide band technology. In the preferred embodiment there is no carrier signal to add or remove and signal processing may be accomplished with the base band frequencies.

In operation, the master transceiver maintains a master clock which runs at a multiple of the data transmission bit rate. The slave transceivers have local clocks which also run at a multiple of the data transmission bit rate and are synchronized to the master clock . The master transceiver manages data transmissions between the slave node device of the networked system.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a wireless network system having a plurality of mobile transceiver devices.

FIG. 2 is a functional block diagram of the physical layer according to an illustrative embodiment of the present invention.

FIG. 3 is a TDMA frame generated by the physical layer of FIG. 2.

FIG. 4a is a block diagram of a transmitter that may be used in the present invention.

FIG. 4b is a block diagram of a drive system of FIG. 4a.

FIG. 5 is a block diagram of a receiver that may be used in the present invention.

FIG. 6a is a typical waveform of two pulses having different pulse repetition frequencies.

FIG. 6b is a typical waveform of a pulse amplitude modulation of a waveform which represents three bits.

FIG. 7 is a typical TDMA frame having variable size data slots.

FIG. 8a is a typical TDMA slot having different pulse repetition frequencies.





FIG. 8b is a typical TDMA slot having two different modulation methods associated with both slots.

## DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

The present invention provides a Time Division Multiple Access (TDMA) system and method that allows sharing a wireless medium which can identify and operate in a variable bit rate environment. The present invention provides a system and method capable of supporting devices with vastly different bandwidth requirements. Some devices, such as television receivers, require high bandwidth data communication. The higher cost associated with a television receiver allows for the design of a television having high data rate modulation techniques. Other devices such as home thermostats have lower bandwidth requirements and require simpler modulation techniques for lower cost connectivity.

The present invention operates within a network which allows devices to operate at different bit rates and employ different modulation techniques and permits sharing of the same wireless medium. Additionally, the transceivers of the present invention are capable of negotiating links between one another which are dependent on environmental characteristics such as noise and reflection. Further still the present invention allows backward compatibility to be designed into the network so that newer devices communicate with older devices. The system preferably works in a base band or ultra wide band environment. However, the system and method may operate in other environments which use carrier signals.

The TDMA system and method of the present invention will be more fully understood by first referring to FIG. 1, which shows a wireless network system 10 comprising a plurality of mobile transceiver devices 12a-12d, also identified as radio devices A-D, wherein each transceiver has a corresponding antenna 14a-14c. One device 12a is acting as a "master" transceiver or device, while the remaining devices 12b, 12c and 12d act as "slave" transceivers or devices. It shall be appreciated by those skilled in the art that the terms transceiver and devices may be used interchangeably. The particular transceiver node 12a-12d which acts as the master device may change depending upon the manner in which the network system 10 is used, and thus the components and hardware for each transceiver 12a-12d are generally the same.

By way of example and not of limitation, the illustrative example of four transceiver devices 12a-12d are shown in network system 10. The master transceiver 12a carries out the operation of managing network communications between transceivers 12b-12d by synchronizing the communications between the transceivers.

Therefore, the master transceiver 12a maintains communication with slave transceivers 12b through 12d. Additionally, the slave transceivers are able to communicate amongst themselves, as illustrated by the typical communications between slave transceiver 12c and 12d. The systems and methods for communications are described in further detail below.

The present invention provides that the master transceiver need not include dedicated communication hardware to provide simultaneous open links between itself and all the slave devices. However, the master device must maintain communications with the slave devices so that all devices on the network are properly synchronized. The present design guarantees that media can be broadcast to many nodes at the same time. It shall be appreciated by those skilled in the art and having the benefit of this disclosure, that the network system 10 may comprise a larger number of transceiver devices, with the actual number of transceiver devices in network system 10 varying depending on the particular application for the system 10.

Referring now to FIG. 2 as well as FIG. 1, a functional block diagram of the "Physical layer" implementation of a transceiver node device 12 in accordance with the present invention is shown. The "Physical layer" as described herein refers to the Physical layer according to the Open Systems Interconnection (OSI) Reference Model.

Each transceiver node device 12a-12d is structured and configured as transceiver device 12 of FIG. 2. The transceiver node device 12 comprises an integrated circuit or like hardware device providing the functions described below. Transceiver device 12 comprises an antenna 14 coupled to a transmitter 16 and a receiver 18. The transmitter 16 is connected to a data modulation unit 20. Transmitter gain control 21 is coupled to transmitter 16. Both the transmitter 16 and the data modulation unit 20 are coupled to an interface to Data Link Layer (DLL) 22. The receiver 18 coupled to the antenna 14 comprises generally an RF front end section 24, a pulse detector 26, a data demodulation or data recovery unit 28. A receiver gain control 30 is included in association with receiver 18.

A framing control unit 32 and a clock synchronization unit 34 are operatively coupled to the receiver 18 and the data modulation unit 20 associated with the transmitter 16. Transmitter 16 and receiver 18 are operatively coupled to antenna 14, preferably through a RF switch (not shown).

Data Link Layer interface 22 comprises circuitry which provides an interface or higher communication exchange layer between the Physical Layer of network 10, as embodied in transceiver 12, and the "higher" layers according to the OSI reference model. The layer immediately "above" the Physical Layer is the Data Link Layer. Output information from the Data Link Layer is communicated to data modulation unit 20 via interface 22. Input data from receiver 18 is communicated to the Data





Link Layer via interface 22.

The data modulation unit 20 comprises circuitry which converts information received from interface 22 into an output stream of pulses. Various forms of pulse modulation may be employed by data modulator 20. One modulation scheme which may be used is on-off keying wherein the presence and absence of pulses respectively represent the "ones" and "zeros" for digital information. In this situation, data modulation unit 20 causes a pulse to be generated at the appropriate bit time to represent a "one", or causes the absence of a pulse to represent a "zero". In another embodiment, pulse amplitude modulation is employed wherein the amplitude of a pulse represents a digital value. The number of bits represented by a pulse depends on the dynamic range and signal-to-noise ratio available. The data modulation method is described in further detail below.

The pulse stream generated by data modulator 20 and transmitted by transmitter 16 is synchronized with a master clock associated with the clock synchronization function 34, and is sent in an appropriate time slot according to a frame definition provided by the framing control unit 32, as described further below. In order to maintain a synchronized network, one device must serve the function of being a clock master and maintaining the master clock for the network 10.

Transmitter 16 is preferably a wide band transmitter device which generates a pulse stream according to output from data modulation unit 20 and which transmits the pulse stream via antenna 14 as a stream of electromagnetic radio frequency (RF) pulses. In the preferred embodiment, data is transmitted via impulses having 100 picosecond risetime and 200 picosecond width, which corresponds to a bandwidth of between about 2.5 GHz and 5 GHz. The transmitter gain control 21 preferably comprises a power control circuit.

Antenna 14 comprises a radio-frequency (RF) transducer and is structured and configured for both transmission and reception. During reception, antenna 14 converts RF pulses into corresponding voltage signals. During transmission antenna 14 converts an electric current containing pulse information into corresponding baseband ultra wide band RF pulses. In one preferred embodiment, antenna 14 is structured and configured as a ground plane antenna having an edge with a notch or cutout portion operating at a broad spectrum frequency at about 3.75 GHz. The structure and configuration of antenna 14 may vary in order to accommodate various frequency spectrum ranges. Antenna 14 may alternatively comprise a "dual antenna" configuration wherein transmission and reception occur from different portions or regions of antenna 14.

Clock synchronization unit 34 includes a clock function (not shown) which maintains a clock or timing device (also not shown). The clock is preferably a conventional voltage controlled oscillating crystal device which operates at a multiple

of the bit rate for the system 10. In the case of the master transceiver 12a, the clock in the clock synchronization unit serves as a master clock for network 10. As noted above, each transceiver node 12a – 12d may act as the master device for the network. A clock recovery function, described further below, is included with receiver 18 wherein timing information from the master clock is recovered.

Framing control unit 32 comprises hardware and/or circuitry which carries out the operations of generating and maintaining time frame information with respect to transmitted data. Framing control unit 32 is utilized by the transceiver node which is acting as the master transceiver by dividing up the transmitted pulse information into "frames". Data transmission between the several node devices 12a – 12d is preferably carried out via a Medium Access Control protocol utilizing a Time Division Multiple Access (TDMA) frame definition.

Subject to the TDMA frame definition, data is transmitted as short RF pulses and is divided into discrete data frames, wherein each data frame is further subdivided into "slots". The frame definition is provided to transceivers 12a – 12d from the Data Link Layer via interface 22. The TDMA frame definition is defined by Medium Access Control (MAC) sublayer software associated with the Data Link Layer. Framing control unit 32 in master transceiver device 12a generates and maintains time frame information through use of a slot having a "Start-Of-Frame" (SOF) symbols, which are used by the slave transceivers 12b – 12d to identify the frames in the incoming data stream.

In the most general terms, the preferred receiver 18 includes a RF front end module 24, pulse detection unit 26, and a data demodulation unit 28. The receiver 18 detects modulated ultra wide band base band pulses generated by the transmitter. The receiver apparatus comprises a RF front end section 28, a pulse detection unit 26, and data recovery unit 24. A more detailed description of the preferred receiver of the present invention is provided below.

Transceiver 12 further includes circuitry for controlling the gain of signals received and transmitted and shown as gain control units 30 and 21, respectively. The transmit gain control unit 21 carries out the operation of controlling the power output of the transmitter 12 and receive gain control unit 30 carries out the operation of controlling the input gain of the receiver 18. The optimized gain for each control unit is dependent on maximizing the power demands for transceiver communications while minimizing the energy consumption of each control unit.

As described in further detail below, the physical layer of the system 10 includes a transmitter 16 and a data modulation unit 20, which is configured to generate a plurality of signals having a variable pulse repetition frequencies and different modulation techniques. The signals generated by the data modulation unit 20 are coupled to a transmitter 16, in which the transmitter 16 generates a pulse





stream according to the data modulation unit 20. The antenna 14 which acts as a transmitting antenna and a receiving antenna is coupled to the transmitter 16. The antenna 14 generates a plurality of ultra wide band base band signals. Additionally, the antenna 14 is capable of receiving ultra wide band base band signals. A receiver 18 coupled to the antenna is configured to detect and demodulate the ultra wide band base band signals. Additionally, the receiver 18 is capable of detecting the variable pulse repetition frequency and different modulation techniques generated by the transmitter 16.

Referring to FIG. 3 there is shown an illustrative TDMA frame useable in the present invention. The TDMA frame 50 is an illustrative frame arrangement provided by the Medium Access Control (MAC) protocol of the present invention. The MAC protocol of the present invention provides services at the MAC sublayer of the Data Link layer according to the Open Systems Interconnection (OSI) reference model. The Logical Link Control (LLC) sublayer is the (upper) portion of the Data Link layer and provides virtual linking services to the Network layer of the OSI reference model. Data transmission framing for transceivers 12a – 12d is provided by the MAC protocol executed within each transceiver on the network. The MAC protocol provides a TDMA frame definition and a framing control function. The TDMA architecture divides data transmission time into discrete data "frames". Frames are further subdivided into "slots".

TDMA frame 50 is an illustrative frame arrangement provided by the MAC layer protocol of the present invention. In general, the MAC layer of the present invention provides the master device 12 with the functions and routines for carrying out the operation of managing each TDMA frame 50 which is communicated in the network system 10. In the preferred embodiment, the TDMA frame 50 comprises a Start-Of-Frame slot 52, a command section 54, and a data slot section 56. The data slot section 56 is further subdivided into a plurality of data slots 60a through 60n.

The architecture of TDMA frame definition 50 provides for isochronous data communications between the master transceiver 12a and the slave transceivers 12b – 12d. It shall be appreciated by those skilled in the art that isochronous data communications refers to processes where data must be delivered within a certain time constraint. Isochronous data communication is supported by frame definition 50 by sharing transmit time so that each transceiver 12a - 12d is permitted to transmit data during a specific allotted time slot.

Asynchronous communication is also supported by the TDMA frame definition 50. It shall be appreciated by those skilled in the art that asynchronous data communications refers to communications in which data can be transmitted intermittently rather than in a steady stream. Within the TDMA frame, slots may be assigned as a random access slot using a technique such as Carrier Sense Multiple

Access with Collision Avoidance (CSMA-CA). For the illustrative CSMA-CA case, the master 12a creates a slot to be used as a random access slot. The master 12a then communicates through the command slot to all random access capable devices that this slot is now available for random access. The master 12a also communicates the start and length of the command slot. The random access slot might be used for all Internet Protocol (IP) devices, for example, such that all IP capable devices will listen to and transmit using only the random access slot reserved for IP traffic. Each IP device on the network listens to this slot. If no communication is detected in this slot for a certain number of frames, this channel is considered "free". A device wishing to transmit waits until the channel is free before transmitting, and then start packet transmission by transmitting in the random access slot for each frame until the transmission was completed. Various schemes for collision avoidance are known in the art.

The Start of Frame slot 52 includes a synchronization slot 58 and a timestamp slot 59. The synchronization slot 58 identifies the start of each new TDMA frame and synchronizes the master device 12a with the slave device 12b through 12d. The synchronization slot 58 from the master transceiver 12a includes a master synchronization code which is generated at least once per frame. Preferably, the master synchronization code comprises a unique bit pattern which identifies the master transceiver as the source of transmission with timing information associated with the master clock in the clock synchronization unit of the master transceiver. By way of example and not of limitation, the master synchronization code uses a 10-bit code comprising "0111111110".

Various encoding schemes known in the art may be used to guarantee that the master synchronization code within synchronization slot 58 will not appear anywhere else in the data sequence of the TDMA frame 50. For example, a common encoding scheme is 4B/5B encoding, where a 4-bit values is encoded as a 5-bit value. Several criteria or "rules" specified in a 4B/5B, such as "each encoded 5-bit value may contain no more than three ones or three zeros" and "each encoded 5-bit value may not end with three ones or three zeros", ensure that a pulse stream will not have a string of six or more ones or zeros. Other encoding techniques known in the art may also be used for master synchronization code including bit stuffing or zero stuffing.

The timestamp slot 59 includes a bit-field which is incremented by a timestamp counter (not shown) in the master device 12a. The timestamp slot 59 permits the master 12a to dynamically reassign the data slot time and length parameters. In operation, the master 12a determines a predetermined time interval required for the modification of the data slot time for data slots 60a through 60n and/or data slot lengths 68a through 68n of the slave devices.





The command section 54 is used by the master transceiver 12a to manage network communications. More particularly, the command section 54 contains a protocol message which is exchanged between the transceiver devices 12a through 12d of network 10 for managing network communications. The flow of protocol messages in the command slot 42 may be governed, for example, by a sequence retransmission request or "SRQ" protocol scheme wherein confirmation of protocol transactions are provided following completion of an entire protocol sequence.

The data slots 60a through 60n are assigned by the master device 12a to requesting slave devices 12b through 12d. Data slots 60a through 60n are further structured and configured to be arranged dynamically and permit the reassigning of the relative start time and the length of the data slots 60a through 60n within the data slot section 56 of the frame 50. This arrangement allows the master device 12a to dynamically manage the usage of the data slot section 56 to optimize the bandwidth capabilities of the transport medium of the network and the devices of the network. Thus, the master device 12a may allocate a wider data slot to a slave device which can utilize a wider bandwidth. Conversely, the master device 12a may also allocate a narrower data slot to a slave device which has more limited bandwidth capabilities. The granularity for data slots 60a through 60n is one (1) symbol. The granularity for data slots 60a through 60n is allocated by the master device 12a.

Each data slot 60a through 60n has a corresponding data synchronization sub-slot 62a through 62n and a data payload sub-slot 64a through 64n. The data payload 64a through 64n contains the encoded actual data or bit information which is transmitted from the source device to the target device. The data synchronization sub-slot 62a through 62n are used by each device for providing timing synchronization signals to a corresponding target devices to accommodate for propagation delays between the source and target devices. Propagation delays vary in length depending on the distance between source and target devices. As described above, the master synchronization code provides timing signals to allow slave devices to synchronize with the master clock of the master device 12a. Likewise, the symbols within the data synchronization sub-slot 62a through 62n are symbols which allow target slave devices to synchronize with corresponding source slave devices using similar synchronization algorithms such as phase offset detectors and controllers. Proper target-to-source device synchronization is fundamental for reliable data communication exchange between the slave device.

Each data slot 60a through 60n has a corresponding slot start time 66a through 66n and corresponding slot length 68a through 68n. The slot start time 66a through 66n corresponds to the time position within the data slot section 56 of the frame at which point the device begins its transmission. The slot length 68a through 68n measured from the slot start time provides the time position within the frame at which

transmission is terminated for the data slot for each frame. The slot lengths 68a through 68n corresponds to the bandwidth allocated to the devices within the data slot section 56 of the frame and may be of varying lengths as assigned by the master device 12a.

The framing control unit 32 in the slave devices 12b through 12d provide framing means such as local counters, correlators, phase lock loop functions, and phase offset detectors and controllers which allow frame synchronization between slave devices 12b through 12d and the master device 12a to be reestablished when the size or length of frame 50 is altered by the master device 12a.

Referring to FIG. 4, there is shown a block diagram of a preferred transmitter system that may be used in the present invention. The transmitting system 70 includes a data modulation unit 20, a transmit gain control unit 21, a transmitter 16, and an antenna 14. The data modulation unit 20 further comprises a pulse amplitude modulation module 72, a pulse repetition frequency module 74 and a transmit module 76.

The pulse repetition frequency module 74 permits varying pulse repetition frequencies to be transmitted. The added benefit of varying pulse repetition frequencies is that it permits transmitting variable bit rates depending on the environmental conditions, such as signal-to-noise ration and/or bit error rate which affect the transceiver signals. Another benefit of varying pulse repetition frequencies is that it reduces the amount of interference generated by a base band transmitter to narrowband receivers. Thus, transmitted signals which fall within the frequency range of the narrowband receiver appear intermittently to the narrowband receiver and thereby reduce interference to the narrowband receiver.

More particularly, the pulse repetition frequency module 74 includes a clock divider which changes the pulse repetition frequency generated by the transmitter. The clock divider is coupled to the transmit module which communicates with the transmitter 16. It shall be appreciated by those skilled in the art having the benefit of this disclosure that a clock divider is capable of dividing clicking signals so that the pulse repetition frequency may be changed at a constant rate or at a variable rate.

The transmit module 76 generates the digital transmit pulse signals which are communicated to the transmitter 16 pulse generator system 78. Additionally, the transmit module 76 is configured to use different modulation techniques such as pulse amplitude modulation (PAM) and on-off keying (OOK) based on channel characteristics. By way of example and not of limitation, two transceivers are communicating to one another and determine that the Bit Error Rate (BER) is too high for the existing communication link. The system and method of the present invention provides for these transceivers to negotiate to use a different modulation technique, such as moving from 8-level PAM to 4-level PAM. Thus, in the





illustrative example, each transceiver configures its respective transmitter to modulate the signal with the new modulation technique.

If the transmit module detects that a signal is modulation by OOK, the OOK signal is communicated directly to the transmitter 16. If the transmit module detects that a signal is modulated by PAM, then the transmit signal is communicated to the PAM module 72 and to the transmitter 16.

It shall be appreciated by those skilled in the art that various forms of pulse modulation may be employed by data modulation unit 20. A typical modulation technique is on-off keying (OOK) wherein the presence and absence of pulses represent the "ones" and "zeros", respectively, of digital information. In this typical situation, the data modulation unit 20 causes a pulse to be generated at the appropriate bit time to represent a "one" or causes the absence of a pulse to represent a "zero."

Another modulation method well known is the art is pulse amplitude modulation. Pulse amplitude modulation allows the amplitude of a pulse to represent a digital value so that the number of bits may be represented by a single base band signal. By way of example and not of limitation, a three bit symbol can be represented with eight levels of pulse amplitude.

The pulse amplitude module 72 receives digital signal to modulate with pulse amplitude modulation. The pulse amplitude modulation module 72 communicates the desired level of amplitude modulation to an digital-analog-converter (DAC). The DAC converts the digital signals to analog signals of various amplitudes and communicates this the drive system, so that the drive system may amplify the pulses. The digital signals are also communicated to the pulse generator system, so that the signals may take the appropriate shape. A clock within the pulse amplitude modulation module 72 ensures that the signals generated by a pulse generator system 78 are properly timed for amplification by a drive system 80.

The modulation technique for the pulse stream generated by the data modulator 20 is synchronized with a master clock associated with the clock synchronization unit 34, and is sent in an appropriate time slot according to a frame definition provided by the framing control unit 32. As previously described, to maintain a synchronized network, one device must serve the function of being a clock master and maintaining the master clock for the network 10.

The transmitter 16 includes a pulse generator system 78 and a drive system 80. The pulse generator system 78 is presented with an input transmit pulse signal from the transmit module 76 and generates pull-up signals and pull-down signals. More particularly, a plurality of pull-up turn-on pulses generated by the Pon module 82, and pull-up turn-off pulses generated by the Poff module 84 are produced by the pull-up circuit. Additionally, a plurality of pull-down turn-on pulses are generated by the Non module 86, and a plurality of pull-down turn-off pulses are generated by the Noff

module 88.

In operation, each module 82, 84, 86 and 88 of pulse generator 42 is presented with edge of an input transmit pulse. The edge of the input pulse is communicated to a plurality of pair of edge delay circuits which generate a plurality of leading edges and trailing edges. Each edge is a delayed by a particular time interval. The trailing edges are generated by inverting a delayed edge. A plurality of NAND gates combine the plurality of pairs of leading and trailing edges. The outputs from the Pon module 82, the Poff module 84, the Non module 86 and the Noff module 88 are communicated to the drive system described below.

Referring to FIG. 4b, there is shown a schematic diagram of a preferred driver system 90, namely, a transistor drive system 90 which may be used by the present invention. The transistor drive system generates the output signal which is communicated to antenna 14 and identified as load 92 in FIG. 4b. The pull-up circuit which generates the output signal excursion submitted to the antenna includes a bipolar pnp transistor 94. The pnp transistor 94 is a pull-up transistor in a common emitter configuration that receives the pull-up signals at its base 95. The pull-down circuit which generates the negative going signal excursion includes a bipolar npn transistor 96. The npn transistor 96 is a pull-down transistor in a common emitter configuration that receives the pull down signals at its base 97. The outputs from the bipolar transistors are capacitively coupled to a load, which is preferably an antenna which radiates the output signal.

As previously described, the output signals generated by the signal generate may operate, for example, between the 2.5 GHZ to 5.0 GHz range. As these operating frequencies, the base-emitter capacitance at each transistor prevent the bipolar transistors from rapidly turning off. To ensure rapid turnoffs the pnp transistor 94 and the npn transistor 96 generate "turn off" signals which discharge the base-emitter capacitance at each transistor 94 and 96. The discharging of the base-emitter capacitive charge turns off the transistors.

Referring to FIG. 5, there is shown a preferred receiver apparatus 18 which may be used by the present system and method. The receiver apparatus 18 comprises an RF front end section 28, a pulse detection unit 26 wherein modulated, ultra wide band pulses are detected, and a data recovery unit 24 wherein clock and data recovery from the detected pulses are carried out. The invention may be embodied in various hardware or circuitry configurations, and is preferably embodied in a single IC device.

The RF front end 28 of the receiver 18 apparatus generally comprises an antenna 14 together with means for filtering and amplifying RF signals received by the antenna 14. The antenna 14 at the RF front end is preferably a ground plane antenna having an edge with a notch or cutout portion operating at a broad spectrum





frequency ranging from about 2.5 gigahertz (GHz) to about 5 GHz, with the center frequency at about 3.75 GHz. An RF switch 102, which may be a conventional antenna switching circuit, is preferably included in association with the antenna 14 to allow the antenna 14 to be shared with the transmitter 16, so that the receiver system of the invention may be implemented together with a transmitter 16 in a transceiver device. The filtering and amplification means preferably comprises one or more band pass filters, such as filters 104 and 106, and one or more low noise, variable gain amplifiers, such as amplifier 108. It shall be appreciated by those skilled in the art that the type, number and configuration of filters and amplifiers used in the front end may vary as required for particular applications of the invention. The RF front end 28 converts the received RF pulses into corresponding voltage signals from which pulse information is detected. Gain control 30 in the form of an automatic gain control loop (AGCL) may also be included with the RF front end.

The pulse detection unit 26 is preferably an envelope detection circuit, and preferably includes a first amplifier, a high (GHz range) operating frequency detector diode, a high pass or band pass filter, a second amplifier, and a comparator. The detector diode is preferably tunnel diode or Schottky diode which provides for envelope detection, rectifies the incoming voltage signals from the RF front end, and provides a power envelope. The filter removes any long term DC or noise components from the signals. The comparator provides threshold detection means and generates pulses when the filtered, rectified voltage signals exceed a predetermined threshold voltage. The shape of the pulsed envelope of the incoming signal can be evaluated from the output of the envelope detection circuit. As in the RF front end, the particular filtering and amplification used in the envelope detection circuit may be varied as required for particular uses of the invention.

The data processing unit 24 retrieves information from the detected pulses output by the pulse detection unit. The data processing unit preferably comprises a clock recovery module 110 for generating master clock timing information from the detected pulse stream, a pulse repetition frequency module 112 for sampling at the right pulse repetition frequency, a phase offset detector 114 for determining delays associated with pulsed data transmission from non-master networked devices, and a data recovery unit 116 for determining digital values from a detected pulse stream according to timing information from the clock recovery module 110 and phase offset information from the phase offset detector 114.

The clock recovery unit 110 generally includes a mask for suppressing selected pulses. Preferably, a pulse stretcher is also included for dilating or stretching pulses to simplify processing by digital logic. A pulse sampler is included in the clock recovery unit to sample the pulses. A correlator is provided for matching incoming pulse trains to the known "master sync code" associated with the master

clocking synchronization unit 34. A synchronization code predictor generates mask signals for suppressing pulses which are not associated with expected pulsed synchronization codes. A phase-locked loop (PLL) synchronizes a local clock in the receiver apparatus to a master clock according to detected or predicted master sync codes. The timing information thus generated is directed to the phase offset detector and data recovery function.

The phase offset detector 114 includes a mask for suppressing selected pulses received from the envelope detector circuit. A pulse stretcher may also be included in the phase offset detector 114 to facilitate subsequent sampling by digital logic. A data header predictor receives output from the correlator in the clock recovery unit 110 and generates mask signals according to detected or expected data header codes in the pulse stream. Timing information from the PLL in the clock recovery unit 110 is directed to an offset detector. The offset detector oversamples the incoming pulse train and determines the phase offset or delay between the phase locked bit clock and the incoming pulses. The phase offset thus determined is provided to the data recovery unit 116.

The data recovery unit 116 uses the phase lock clock information from the PLL and the phase offset from phase offset detector 114 to sample the incoming pulse stream having a variable pulse repetition frequency at the appropriate, phase offset corrected times, and provide a digital value for each incoming symbol in the pulse stream. To determine the pulse repetition frequency in a variable pulse repetition frequency environment, the receiver includes a divider circuit 118 operatively coupled to PLL in the clock recovery function100 and to a digitally controlled delay circuit or sampling timer circuit. In a variable pulse repetition frequency environment, the divider circuit 118 provides the function of determining the sampling rate for signals submitted to data recovery unit 116. The divider circuit divides the rate of data sampling according to the sampling rate detected by PLL. The divider circuit 118 communicates the data sampling rate to the delay circuit or sampling circuit. The delay or sampling circuit is also coupled to the phase offset detector 114. The sampling circuit or delay circuit provides the function of determining when to sample the incoming data signals according to output generated by both the divider circuit and the phase offset detector 114.

An analog-to-digital converter (ADC) in the data recovery function receives the analogue output from the envelope detector and decodes it to digital values according to the determined sample timing. A decoder 119 converts the digital values from the ADC to symbols. For different modulation method such as pulse amplitude modulation or on-off keying, the decoder 119 is capable of detecting different threshold levels which identify the particular modulation method. In the case of on-off keying, the presence or absence of a pulse at the sampled time corresponds to a





digital "one" or "zero". For on-off keying modulation, ADC may be a one-bit ADC, or alternatively, a comparator circuit. In the case of pulse amplitude modulation, decoder 119 utilizes quantization levels to determine the output value per measured voltage level. In one embodiment wherein pulse amplitude modulation is used, eight voltage levels are used to produce a three-bit value. The symbol output is delivered to higher protocol layers of the network system.

Referring to FIG. 6a, as well as FIG. 1 and FIG. 3, there is shown an illustrative example of two output signals associated with antenna 14 transmitting at a variable pulse repetition frequency. The illustrative example shows two signals being transmitted at two different pulse repetition frequencies. The first typical signal has a pulse repetition frequency is identified as $f_1$ 120 and is represented by the base band pulses having dotted lines. The second typical signals have a particular pulse repetition frequency identified as $f_2$ 122. Preferably, the baseband transceiver of the present invention is configured to transmit and receive different pulse repetition frequencies for each slot in the TDMA frame 50. As previously described, the pulse repetition frequency may be changed at a constant rate or at a variable rate.

Referring to FIG. 6b, as well as FIG. 1, there is shown an illustrative example of possible output signals representing a three-bit sequence. The output signals are transmitted by antenna 14 employing pulse amplitude modulation. In pulse amplitude modulation the information is conveyed by the amplitude of the pulse. The illustrative example shows a signal having a maximum amplitude 130 representing a three-bit sequence, 1 1 1. The illustrative example also shows a signal having a minimum amplitude 132 representing a three-bit sequence, 0 0 0. The various PAM levels between the minimum amplitude sequence 130 and the maximum sequence 132 provide eight different amplitude levels which represent one of the eight possible three-bit sequences.

Referring to a typical TDMA frame 140 of FIG. 7, as well as FIG. 3, FIG. 2 and FIG. 1, there is shown the TDMA frame 140 which communicates different modulation methods at variable pulse repetition frequencies for network system 10. It shall be appreciated that the TDMA frame 140 is substantially similar to TDMA frame 50, with the exception that the data slots in the data slot section 12a through 12d communicate variable size data slots to the devices in the typical network.

A SOF section 142 which includes a synchronization slot 44 . The synchronization slot 144 identifies the start of each new TDMA frame and synchronizes the master device 12a with the slave device 12b through 12d. In its preferred embodiment, the master device 12a transmits a unique synchronization symbol within the synchronization slot 144, which does not appear anywhere else within the frame to identify the start of each new frame. The unique synchronization symbols are used by each of the slave devices 12b through 12d on the network to

ascertain the beginning of each from the incoming data stream.

The network is synchronized by the clock 13 in the master transceiver and clock recovery module in the slave transceivers. Each node device in the network system maintains a clock running at a multiple of the bit rate of transmission. The clock synchronization unit 34 in the master device maintains the master clock 13 for the network. At least once per frame, the clock synchronization unit 34 issues a "master synchronization code" in the synchronization slot 144. The master sync code is typically a unique bit pattern which identifies the sender as the clock master.

The clock synchronization unit 34 in the slave devices 12b through 12d on the network 10 carries out the operation of recovering clock information from the incoming data stream and synchronizing the slave device to the master device. It shall be appreciated by those skilled in the art having the benefit of this disclosure that the synchronization is accomplished using one or more correlators which identifies the master synchronization code and a phase or delayed locked loop mechanism. By providing a common network clock on the master device, with slave devices synchronizing their local clocks to that of the master clock, support for synchronous, isochronous and asynchronous communication is provided. Time reference between all device nodes is highly accurate eliminating most latency and timing difficulties in isochronous communication links.

The SOF section 142 also includes a timestamp slot 146. The timestamp slot 146 is a bit-field that is incremented by modulo-N timestamp counter located on the master device, where N is chosen to be sufficiently larger than the time required to perform all anticipated slot-reorganization tasks. The modulo-N counter rolls over to zero after reaching N-1. Each slave device 12 through 12d keeps a local copy of the timestamp counter which is also incremented for each frame and is used during frames when the SOF section 142 is determined to be corrupted. The purpose of the local timestamp counter is to allow the local device to recognize the frame time even if the SOF section 142 gets corrupted in one or more frames.

The command section 148 is used for sending, requesting and authorizing commands between the master transceiver 12a and the slave transceivers 12b through 12d of the network. The master transceiver 12a uses the command slot for ascertaining which slave transceivers are on-line, off-line or engaged in data transfer. The master transceiver 12a uses the command slot for ascertaining which slave transceivers are online, off-line, or engaged in data transfer. The master transceiver 12a further uses the command slot for authorizing data transmission request from each of the slave transceivers.

The slave transceivers 12b through 12d use the command slot for requesting data transmission and indicating its start-up (on-line) state, engaged state, or shut-down (off-line) state. The data slots are used for data transmission between the node





devices of the network. Generally, each transmitting device of the networks is assigned one or more corresponding data slots within the frame in which the device may transmit data directly to another slave device without the need for a "store and forward" scheme as is presently used in the prior art.

A slave device that is in the "online" state is ready to send or receive data from the other devices on the network 10. Additionally, a slave device is in the "online" state if it is not currently engaged in communication with other slave devices. A slave device is "engaged" when the device is currently communicating with one or more slave devices. For example, where a source slave device is transmitting audio signal data to a target slave device, both the source and target slave device are in the "engaged" state.

By way of example and not of limitation, more detailed information regarding TDMA frame 140 are described by referring to Table 1 which describes typical operating parameters for each device in the network 10. More particularly, Table 1 describes the communications between devices 12a through 12d. The first column of Table 1 identifies the devices in communication. The notation A>B provides that transceiver A, 12a, directs communications to transceiver B, 12b.

TABLE 1.

| Device | Bits/Symbol | Symbols/Sec | Max. Data Rate |
|---|---|---|---|
| A>B | 3 | 20 Million | 60 Mbps |
| A>C | 2 | 10 Million | 20 Mbps |
| B>A | 3 | 20 Million | 60 Mbps |
| C>A | 2 | 10 Million | 20 Mbps |
| C>D | 1 | 20 Million | 20 Mbps |
| D>C | 1 | 20 Million | 20 Mbps |

The second column with the heading bits/symbol provides the number of bits that represented by the communicated baseband signal. For example, if three (3) bits/symbol are identified, then for each baseband signal communicated, three (3) bits of information are communicated. To accomplish the three bits per symbol communications, three-bit pulse amplitude modulation is employed. As previously described, three-bit pulse amplitude modulation provides eight different amplitude level which represent one of the eight (8) possible three-bit outputs.

The third column with the heading symbols/sec provides the number of symbols that are communicated by the baseband transceiver for each second of communications. The numbers of symbols communicated per second is dependent on the pulse repetition frequency employed by the network. For example, the pulse repetition frequency to communicate 20 million symbols per second from transceiver

A, 12a, to transceiver B, 12b, has a pulse repetition frequency of 20MHz. To generated communications on the order of 10 million symbols per second, the number of pulses of symbols communicated is one-half (1/2) of 20 million symbols per second or a pulse repetition frequency of 10 MHz.

The fourth column with the heading maximum data rate combines the bits/symbol column data and symbols/second column data to generate a value of the million bits per second (Mbps). For example, the maximum data rate for the row 1 information is based on multiply 3 bits/symbol by 20 million symbols/second to generate 60 Mbps. A similar calculation for each of the remaining devices is performed to obtain the maximum data rate. It shall be appreciated by those of ordinary skill in the art that the actual data rates are less than the maximum data rate from the fourth column because the TDMA frame is shared with other transceivers in the network.

It shall be appreciated by those with ordinary skill in the art having the benefit of this disclosure that each transceiver 12a through 12b shares the ability to encode and decode symbols employing 3-bit PAM, 2-bit PAM, 1-bit PAM and OOK at a symbol rate that is dependent on the pulse repetition frequency. The use of each of the particular modulation methods described and of the particular pulse repetition frequencies described are not intended to be restrictive, rather they are intended to provide a description of a working embodiment for the present invention.

Referring back to FIG. 7 and Table 1, TDMA frame 140 presents the data slots 150 and 152 for communications between transceiver A, 12a, and transceiver B, 12b. The data slot 150 and 152 have a particular slot start time and slot length. The typical slot length for communications from transceiver A to transceiver B is the same as the slot length for communications from transceiver B to transceiver A. Data slots 154 and 156 provide communications between transceiver A, 12a, and transceiver C, 12c. It shall be appreciated by those skilled in the art having the benefit of this disclosure that the slot length for data slots 154 and 156 is longer than the longer than the slot length for data slots 150 and 152. Data slots 158 and 160 provide the data slot communications between transceiver C, 12c, and transceiver D, 12d. It shall be appreciated by those of ordinary skill in the art having the benefit of this disclosure that the master device, 12a, maintains communications by synchronizing the communications between transceivers 12a through 12d. Additionally, that each of the data slots 158 and 160 has a particualr start time and slot length. The slot length for data slots 158 and 160 is smaller than the slot length of data slots 154 and 156. Further, the slot length for data slots 158 and 160 is larger than the slot length of data slots 150 and 152.

Referring back to Table 1, the slot communications between transceiver A, 12a, and transceiver B, 12b, is 3 bits per symbol at 20 million symbols per second to





produce a maximum data communication rate of 60 Mbps. The 3-bit per symbol modulation is supported by pulse amplitude modulation. The slot communications between transceiver A, 12a, and transceiver C, 12c, is 2 bits per symbol at 10 million symbols per second to produce a maximum data communication rate of 20 Mbps. The 2-bit per symbol modulation is supported by 2-bit pulse amplitude modulation. The slot communications between transceiver C, 12c, and transceiver D, 12d, is 1 bit per symbol at 20 million symbols per second to produce a maximum data communication rate of 20 Mbps. It shall be appreciated by those of ordinary skill in the art, that the 1-bit modulation method may be perform by 1-bit pulse amplitude modulation or on-off keying.

Referring to FIG. 8a, as well as FIG. 7, FIG. 3 and FIG. 1, there is shown a typical illustrative example of the timing for two TDMA slots having different pulse repetition frequencies. A first typical TDMA slot 180 and second typical TDMA slot 182 provides communications within a data slot, such as shown in FIG. 7.

To accommodate variable pulse repetition frequencies for each TDMA slot, the master sync code synchronizes communications between transceiver devices using a clock synchronization unit 34 operating at a nominal pulse repetition frequency that the system 10 will support. The transmitter unit 16 and receiver 18 are capable of frequency multiplying the clock from the clock synchronization unit 34 to support higher pulse repetition frequencies. The pulse repetition frequencies employed may be depend on the devices particular bandwidth demands, noise constraints, or signal reflection.

Client bit clock_1, 184, provides the timing for the pulse repetition frequency associated with TDMA Slot N+1, 182. The signals transmitted by TDMA slot 182 are transmitted during the leading edge of client bit clock_1, 184. Client bit clock_2 186 provides the timing for the pulse repetition frequency associated with TDMA slot N 180. The signals transmitted by TDMA Slot N 180 are transmitted during the leading edge of client bit clock_2 186. The pulse repetition frequency for TDMA Slot N, 180, is two times greater, i.e. faster, that the pulse repetition frequency for TDMA Slot N+1, 182. The pulse repetition frequency for TDMA Slot N, 180, and TDMA Slot N+1, 182, is identified by the frequency pulses, identified by arrows, shown in line 188.

Referring to FIG. 8b there is shown a typical example of the transceiver timing having a different modulation method for each TDMA slot. A client bit clock 190 provides the timing for the two typical TDMA slot in the data slot section of TDMA frame 140 or TDMA frame 70. The two typical TDMA frames are identified as TDMA Slot N, 192, and TDMA Slot N+1, 194. It shall be appreciated by those skilled in the art having the benefit of this disclosure that for TDMA Slot N, 192, the signal transmitted employs pulse amplitude modulation as depicted by the symbols in

line 196. The timing for each of the pulses having a different amplitude is established by the client bit clock 190. Additionally, it shall be appreciated by those skilled in the art that for TDMA Slot N+1 194 the signal transmitted employs on-off keying as depicted by the symbols in line 196. Again, the timing for each of the pulses operating with on-off keying is established by the client bit clock 190.

The techniques described above use different bit pulse repetition frequencies and modulation techniques for baseband communications or ultra-wide-band communications. An additional modulation technique referred to as pulse-position modulation is well known in the art and may also be employed with the present system and method. During pulse position modulation, pulses are transmitted at some basic symbol frequency, e.g. 20 MHz. At 20MHz symbol repetition frequency suggests that pulses be spaced 50 nanoseconds apart. A pulse falling exactly where expected may indicate a binary "1", while a pulse delayed by some small delta time may indicate a binary "0".

The system of the present invention may be broadened for use with carrier signals and other modulation technique. Therefore, while embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.





## CLAIMS

What is claimed is:

1. A network communication system, comprising:

a first device having a first data bandwidth requirement, said first device configured to transmit and receive data at different data rates;

a second device having a second data bandwidth requirement, said second device configured to transmit and receive data at different data rates and configured to communicate with said first device; and

a master transceiver configured to manage data communications between said first device and said second device.

2. The network communication system of claim 1, wherein said communication between said first device and said second device is configured to be performed in a wireless environment.

3. The network communication system of claim 1, wherein said transmitted and received data rates between said first device and said second device varies as a function of noise or reflection.

4. The network communication system of claim 1, wherein said communications between said first device and said second device is configured to operate in an ultra wide band environment.

5. A network communication system, comprising:

a first slave transceiver configured to communicate a plurality of TDMA data packets at different data rates;

a second slave transceiver configured to communicate a plurality of TDMA data packets at different data rates to said first slave transceiver; and

a master transceiver configured manage data communications between said first slave transceiver and said second slave transceiver.

6. The network communication system as recited in claim 5 wherein said master transceiver is further configured to synchronize communications between said first slave transceiver and said second slave transceiver.

7. The network communication system as recited in claim 5 further comprising a third transceiver in communications with said master transceiver, said third transceiver configured to communicate a plurality of TDMA data packets at different data rates.

8. The network communication system as recited in claim 5, wherein said communication between said first slave transceiver and said second slave transceiver is configured to be performed in a wireless environment.

9. The network communication system as recited in claim 5, wherein said plurality of TDMA data packet communication between said first slave transceiver and said second slave transceiver varies as a function of noise or reflection.

10. The network communication system as recited in claim 5 wherein said communication between said first slave transceiver and said second slave transceiver is configured to operate in an ultra wide band environment.

11. A master transceiver configured to transmit ultra wide band base band pulses, comprising:

at least one slave transceiver in communication with the master transceiver; and

a framing control unit housed by said master transceiver, said framing control unit configured to generate and maintain a plurality of TDMA frames, each of said plurality of TDMA frames having a plurality of slots, each of said plurality of slots having a start of frame slot, said start of frame slot configured to identify each of said plurality of TDMA frames to said at least one slave transceiver.

12. The master transceiver recited in claim 11 further comprising a Medium Access Control protocol in communication with said framing control unit, said Medium Access Control protocol configured to define each of said plurality of TDMA frames.

13. The master transceiver recited in claim 11 wherein said communications between said master transceiver and said at least one slave transceiver is configured to provide for isochronous data communications.

14. The master transceiver recited in claim 11 wherein said communications between said master transceiver and said at least one slave transceiver is configured to provide for asynchronous data communications.

15. The master transceiver recited in claim 11 wherein said start of frame slot generated by said master transceiver further comprises a synchronization slot configured to synchronize communications between said master transceiver and said at least one slave transceiver.

16. The master transceiver recited in claim 15 wherein said start of frame slot generated by said master transceiver further comprises a timestamp slot which is configured to permit said master transceiver to modify each of said plurality of TDMA frames at a predetermined time interval.

17. A transceiver, comprising:

a data modulation unit configured to generate a plurality of signals having variable pulse repetition frequencies and different modulation techniques;

a transmitter coupled to said data modulation unit, said transmitter configured to generate a pulse stream according to said data modulation unit;





an antenna coupled to said transmitter, said antenna configured to transmit a plurality of ultra wide band base band signals; and

a receiver configured to detect and demodulate said ultra wide band base band signals.

18. The transceiver recited in claim 17, wherein said data modulation unit comprises a pulse repetition frequency module configured to permit varying pulse repetition frequencies to be transmitted.

19. The transceiver recited in claim 17, wherein said data modulation unit comprises a transmit module configured to generate said plurality of signals which are communicated to said transmitter.

20. The transceiver recited in claim 19, wherein said transmit module is configured to modulate signals for different modulation techniques.

21. The transceiver recited in claim 17, where said transmitter further comprises a pulse generator system configured to generate a plurality of pull-up signals and a plurality of pull-down signals.

22. The transceiver recited in claim 21, wherein said transmitter further comprises a transistor drive system, said transistor drive system configured to communicate said plurality of pull-up signals and said plurality of pull-down signals to said antenna.

23. The transceiver recited in claim 17, wherein said receiver further comprises a front end configured to receive and amplify said ultra wide band base band signal generated by said transmitting antenna.

24. The transceiver recited in claim 23 wherein said receiver further comprises a pulse detection unit coupled to said front end, said pulse detection unit configured to detect a plurality of pulse detection pulses from said received and amplified ultra wide band base band signals.

25. The transceiver recited in claim 24 wherein said receiver further comprises a data processing unit coupled to said pulse detection unit, said data processing unit configured to retrieve a plurality of data from said plurality of pulse detection pulses.

26. The transceiver recited in claim 25 wherein said data processing unit further comprises a divider circuit hosed within said data processing unit, said divider circuit configured to provide the pulse repetition frequency for sampling by said data processing unit.

27. The transceiver recited in claim 25 wherein said data processing unit further comprises a decoder housed within said data processing unit, said decoder configured to detect different modulation techniques.

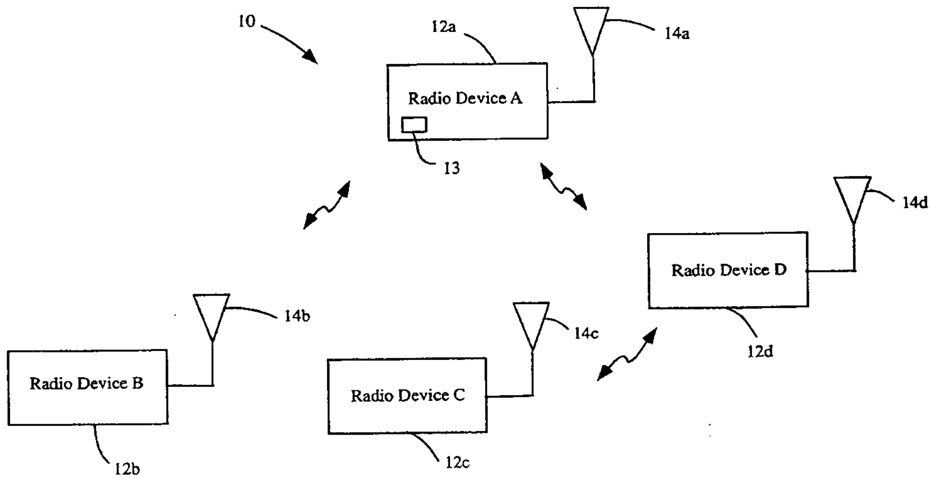

10
12a
Radio Device A
14a
13
Radio Device D
14d
12d
Radio Device B
14b
12b
Radio Device C
14c
12c

Fig. 1







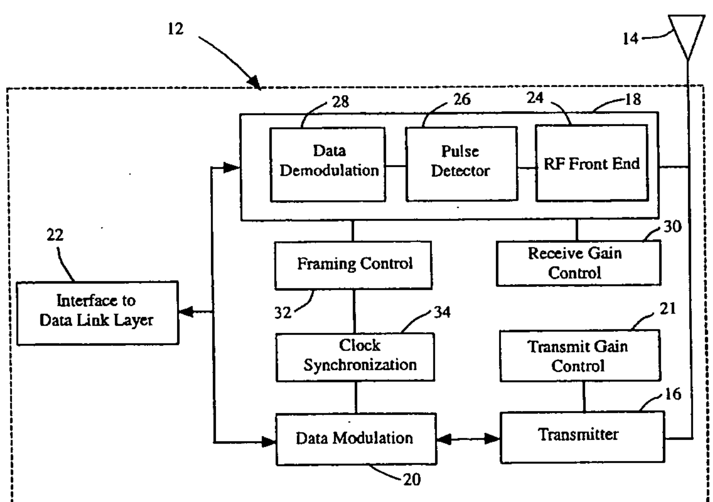

12
14
28
26
24
18
Data Demodulation
Pulse Detector
RF Front End
22
Interface to Data Link Layer
Framing Control
32
Receive Gain Control
30
Clock Synchronization
34
Transmit Gain Control
21
Data Modulation
20
Transmitter
16

Fig. 2

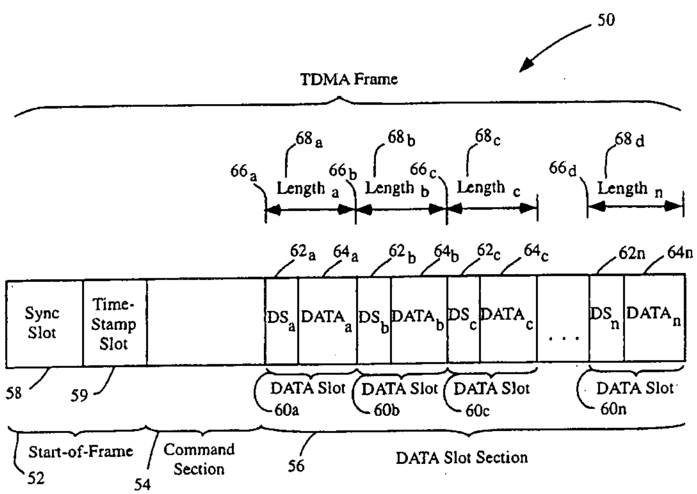

50
TDMA Frame
$68_a$
$68_b$
$68_c$
68 d
$66_a$
$66_b$
$66_c$
$66_d$
Length a
Length b
Length c
Length n
$62_a$
$64_a$
$62_b$
$64_b$
$62_c$
$64_c$
62n
64n
Sync Slot
Time-Stamp Slot
$DS_a$
$DATA_a$
$DS_b$
$DATA_b$
$DS_c$
$DATA_c$
$DS_n$
$DATA_n$
58
59
DATA Slot
60a
60b
60c
60n
Start-of-Frame
52
Command Section
54
56
DATA Slot Section

Fig. 3





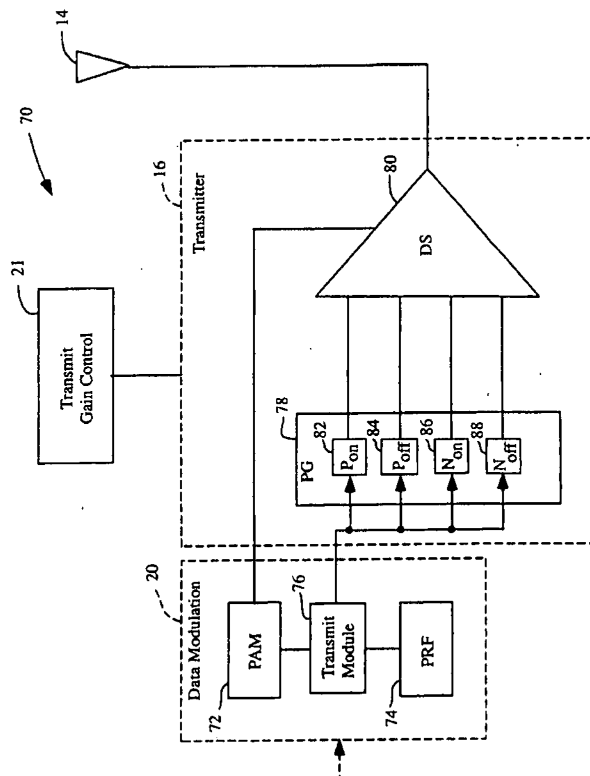
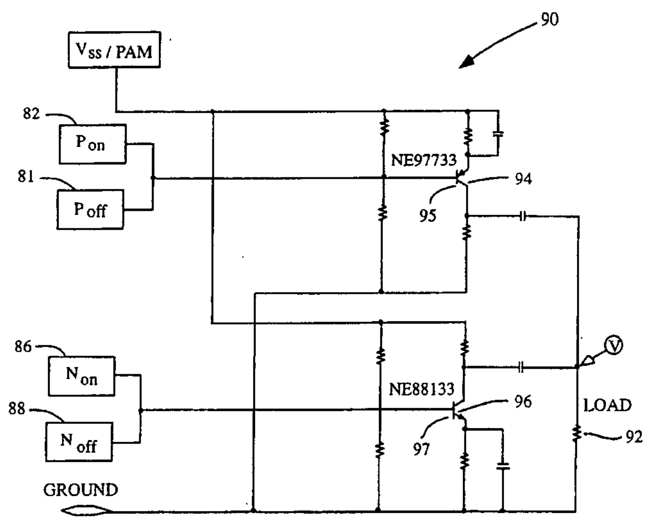

14
70
21
Transmit Gain Control
16
Transmitter
80
DS
78
PG
82
$P_{on}$
84
$P_{off}$
86
$N_{on}$
88
$N_{off}$
20
Data Modulation
PAM
76
Transmit Module
PRF
72
74

Fig. 4A



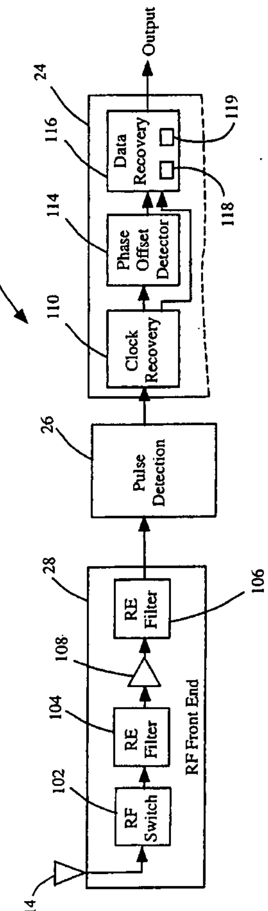
90
$V_{ss}$ / PAM
82
$P_{on}$
81
$P_{off}$
NE97733
94
95
86
$N_{on}$
88
$N_{off}$
NE88133
96
97
LOAD
92
GROUND


Fig.4B









Output
24
116
Data Recovery
119
118
114
Phase Offset Detector
18
110
Clock Recovery
26
Pulse Detection
28
RE Filter
106
108
104
RE Filter
RF Front End
102
RF Switch
14


Fig. 5

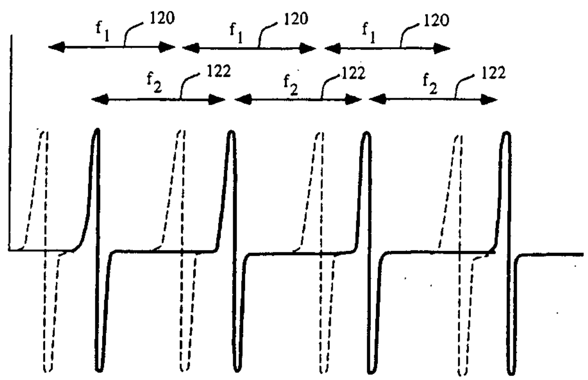



Fig. 6A

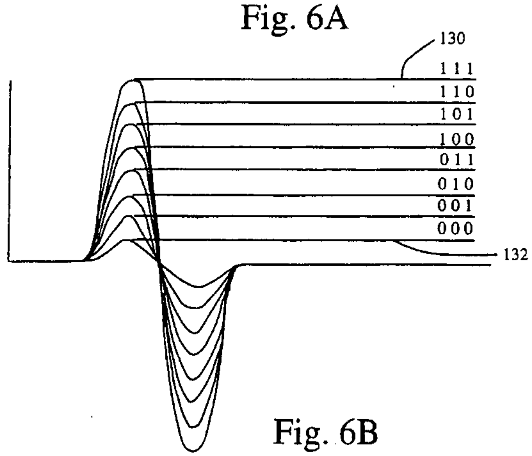



Fig. 6B





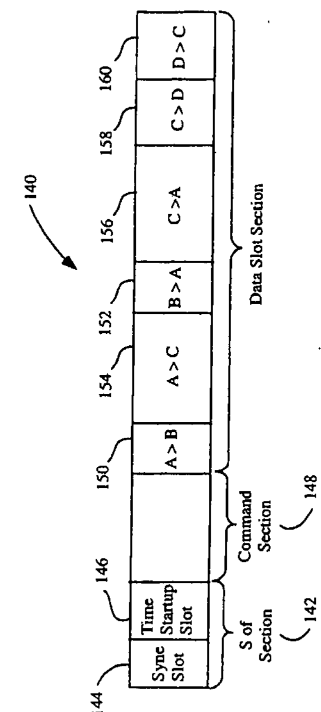



Fig. 7

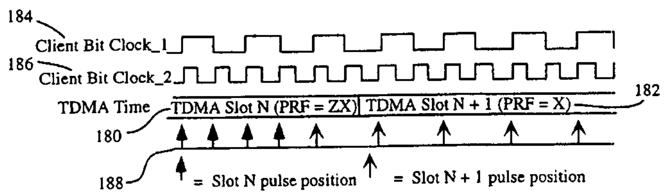



Fig. 8A

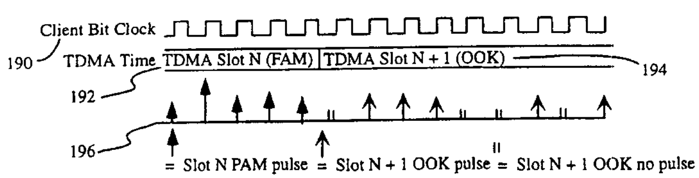



Fig. 8B



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 January 2002 (03.01.2002)

PCT

(10) International Publication Number
WO 02/001735 A3

(51) International Patent Classification⁷: H04L 12/28, 12/56

(21) International Application Number: PCT/US01/19907

(22) International Filing Date: 21 June 2001 (21.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/603,310 21 June 2000 (21.06.2000) US

(71) Applicant: PULSE-LINK, INCORPORATED [US/US]; Suite 8,, 9155 Brown Deer Road, San Diego, CA 92121 (US).

(72) Inventors: **SPARRELL, Carlton**; 2100 Oberlin Street, Palo Alto, CA 94306 (US). **AIELLO, Roberto**; 470 Alger Drive, Palo Alto, CA 94306 (US). **ROGERSON, Gerald**; 2204 Hermosa Court, Morgan Hill, CA 95037 (US). **HO, Minnie**; 3427 Thomas Drive, Palo Alto, CA 94303 (US).

(74) Agent: D'ALESSANDRO, Kenneth; Sierra Patent Group, Ltd., P.O. Box 6149, Stateline, NV 89449 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

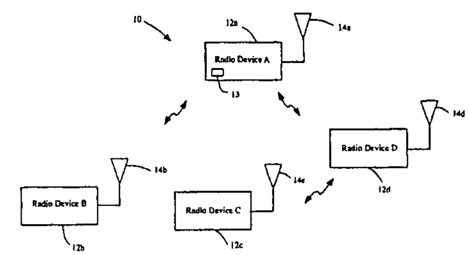
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
17 October 2002

*[Continued on next page]*

(54) Title: WIRELESS TDMA SYSTEM AND METHOD FOR NETWORK COMMUNICATIONS




(57) Abstract: The present invention describes a network communication system which includes a first slave transceiver configured to communicate a plurality of TDMA data packets at different data rates to a second slave transceiver. The second slave transceiver is also configured to communicate a plurality of TDMA data packets at different data rates to the first slave transceiver. A master transceiver manages data communications between the first slave transceiver and the second slave transceiver. Each transceiver includes a data modulation unit, a transmitter, an antenna, and a receiver. The data modulation unit is configured to generate a plurality of signals having variable pulse repetition frequencies and different modulation techniques. The transmitter is coupled to the data modulation unit and the transmitter is configured to generate a pulse stream according to the data modulation unit. The transmitting antenna is coupled to the transmitter and the transmitting antenna is configured to transmit a plurality of ultra wide band baseband signals. The receiver is configured to detect and demodulate said ultra wide band base band signals operating at variable pulse repetition frequencies and having different modulation methods.

WO 02/001735 A3

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/19907

**A. CLASSIFICATION OF SUBJECT MATTER**
IPC 7 H04L12/28 H04L12/56

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, PAJ, EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5 355 374 A (LUSK ALAN ET AL)<br>11 October 1994 (1994-10-11)<br>column 1, line 9 -column 3, line 8<br>column 3, line 33 -column 4, line 2<br>column 7, line 49 -column 8, line 47<br>claim 1 | 1,2,4,5,<br>7,8,10 |
| Y<br>A | | 3,6,9<br>11,17 |
| | --- | |
| X | EP 0 307 962 A (NIPPON ELECTRIC CO)<br>22 March 1989 (1989-03-22)<br>abstract<br>column 1, line 3 -column 4, line 43<br>column 5, line 40 -column 6, line 27<br>column 7, line 20 -column 9, line 12 | 1,2,4,5,<br>7,8,10 |
| Y<br>A | | 3,6,9<br>11,17 |
| | --- | |
| | -/-- | |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 19 July 2002 | 26/07/2002 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Vaskimo, K |

Form PCT/ISA/210 (second sheet) (July 1992)

## INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/19907

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 4 887 266 A (OWEN LYNDON N ET AL) 12 December 1989 (1989-12-12)<br>column 1, line 5 -column 3, line 33<br>column 4, line 6 - line 15<br>column 5, line 48 -column 6, line 14<br>column 7, line 20 - line 54 | 11-16 |
| Y | | 6 |
| A | | 1,5,17 |
| X | WO 91 07030 A (MOTOROLA INC) 16 May 1991 (1991-05-16)<br>page 1, line 13 -page 2, line 24<br>page 4, line 19 - line 25<br>page 5, line 21 - line 32<br>claims 1,2 | 11-16 |
| Y | | 6 |
| A | | 1,5,17 |
| X | US 5 473 668 A (NAKAHARA TORU) 5 December 1995 (1995-12-05)<br>abstract<br>column 1, line 6 -column 2, line 31<br>column 3, line 20 - line 43 | 11-16 |
| Y | | 6 |
| A | | 1,5,17 |
| X | US 5 909 469 A (SCHRAMM PETER ET AL) 1 June 1999 (1999-06-01)<br>column 1, line 6 -column 3, line 34<br>column 3, line 66 -column 4, line 61 | 17-27 |
| A | | 1,5,11 |
| X | US 5 940 452 A (RICH RANDALL WAYNE) 17 August 1999 (1999-08-17)<br>column 1, line 6 -column 3, line 41<br>column 24, line 17 - line 53<br>column 25, line 33 -column 26, line 9<br>column 27, line 41 -column 28, line 3 | 17-27 |
| A | | 1,5,11 |
| X | US 5 926 501 A (HILL CASEY ET AL) 20 July 1999 (1999-07-20)<br>column 1, line 5 -column 2, line 26<br>column 2, line 62 -column 3, line 67<br>column 6, line 51 -column 7, line 37 | 17-27 |
| A | | 1,5,11 |
| X | WO 97 21294 A (AIRONET WIRELESS COMMUNICATION) 12 June 1997 (1997-06-12)<br>abstract<br>page 1, line 9 -page 12, line 30<br>claims 14-16,21,22 | 17-27 |
| A | | 1,5,11 |

-/--



## INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/19907

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | EP 0 825 794 A (LUCENT TECHNOLOGIES INC) 25 February 1998 (1998-02-25)<br>abstract<br>page 2, line 5 -page 3, line 14<br>page 3, line 34 - line 51<br>page 4, line 21 - line 42 | 3,9 |
| A | | 1,5 |
| Y | US 6 055 411 A (ISHIDA KAZUHITO ET AL) 25 April 2000 (2000-04-25)<br>column 1, line 6 -column 2, line 13<br>column 2, line 45 - line 55 | 3,9 |
| A | | 1,5 |

## INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 01/19907

**Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)**

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.





**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-10

A communication system with a plurality of devices, where each device has a bandwidth requirement, where each device is configured to transfer data at different data rates, and where a master device manages communications between said plurality of devices.

2. Claims: 11-16

A master device in communication with at least one slave device, where said master comprises a framing control unit to generate a plurality of TDMA frames, where each frame has a plurality of slots, where each plurality of slots has a start of frame slot, and said start of frame slot is configured to identify said frames to said at least one slave device.

3. Claims: 17-27

A transceiver comprising as modulator capable of operating at plural transmision rates and using different modulation techniques, a transmitter, an antenna, and a receiver.

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/19907

| Patent document cited in search report | | Publication date | Patent family member(s) | | Publication date |
|---|---|---|---|---|---|
| US 5355374 | A | 11-10-1994 | US | 5351240 A | 27-09-1994 |
| | | | US | 5349580 A | 20-09-1994 |
| EP 0307962 | A | 22-03-1989 | JP | 1078541 A | 24-03-1989 |
| | | | JP | 1954076 C | 28-07-1995 |
| | | | JP | 6081113 B | 12-10-1994 |
| | | | AU | 623089 B2 | 07-05-1992 |
| | | | AU | 2246088 A | 23-03-1989 |
| | | | CA | 1286429 A1 | 16-07-1991 |
| | | | DE | 3886149 D1 | 20-01-1994 |
| | | | DE | 3886149 T2 | 16-06-1994 |
| | | | EP | 0307962 A2 | 22-03-1989 |
| | | | US | 4937818 A | 26-06-1990 |
| US 4887266 | A | 12-12-1989 | AU | 594057 B2 | 01-03-1990 |
| | | | AU | 5812386 A | 18-11-1986 |
| | | | EP | 0259315 A1 | 16-03-1988 |
| | | | WO | 8606571 A1 | 06-11-1986 |
| | | | JP | 62502651 T | 08-10-1987 |
| | | | NO | 865227 A | 22-12-1986 |
| WO 9107030 | A | 16-05-1991 | AU | 7741291 A | 31-05-1991 |
| | | | CS | 9005201 A3 | 18-03-1992 |
| | | | HU | 58172 A2 | 28-01-1992 |
| | | | PL | 287486 A1 | 29-07-1991 |
| | | | WO | 9107030 A1 | 16-05-1991 |
| US 5473668 | A | 05-12-1995 | JP | 7087558 A | 31-03-1995 |
| US 5909469 | A | 01-06-1999 | NONE | | |
| US 5940452 | A | 17-08-1999 | CN | 1155793 A ,B | 30-07-1997 |
| | | | GB | 2307831 A ,B | 04-06-1997 |
| | | | JP | 9181665 A | 11-07-1997 |
| | | | KR | 211476 B1 | 02-08-1999 |
| | | | SG | 47195 A1 | 20-03-1998 |
| US 5926501 | A | 20-07-1999 | WO | 9826526 A1 | 18-06-1998 |
| WO 9721294 | A | 12-06-1997 | US | 5950124 A | 07-09-1999 |
| | | | AU | 710939 B2 | 30-09-1999 |
| | | | AU | 1328997 A | 27-06-1997 |
| | | | CA | 2210792 A1 | 12-06-1997 |
| | | | EP | 0812503 A2 | 17-12-1997 |
| | | | JP | 10511835 T | 10-11-1998 |
| | | | WO | 9721294 A2 | 12-06-1997 |
| | | | US | 6132306 A | 17-10-2000 |
| | | | US | 6128512 A | 03-10-2000 |
| EP 0825794 | A | 25-02-1998 | US | 6075777 A | 13-06-2000 |
| | | | CA | 2209351 A1 | 21-02-1998 |
| | | | EP | 0825794 A2 | 25-02-1998 |
| | | | JP | 3096665 B2 | 10-10-2000 |
| | | | JP | 10094042 A | 10-04-1998 |
| US 6055411 | A | 25-04-2000 | JP | 9289675 A | 04-11-1997 |
| | | | CN | 1166761 A ,B | 03-12-1997 |